What is claimed is:

1. A bipolar device comprising:

a base;

an emitter above said base, wherein said emitter has a T-shape with a lower section and an upper section that is wider than said lower section;

spacers adjacent said lower section of said emitter and beneath said upper section of said emitter; and

a silicide layer adjacent said spacers and beneath said upper section of said emitter.

2. The device in claim 1, further comprising a dielectric structure over said base and beneath said spacers.

3. The device in claim 2, wherein said base is wider than said dielectric structure.

4. The device in claim 1, wherein said spacers separate said emitter from said silicide.

5. The device in claim 1, wherein said base comprises:

an intrinsic base; and

an extrinsic base above said intrinsic base.

6. The device in claim 1, wherein said spacers comprise insulators.

7. The device in claim 1, wherein said silicide layer comprises a salicide.

8. A transistor device comprising:

a lower semiconductor structure having a first-type impurity;

a middle semiconductor region above said lower semiconductor structure, said middle semiconductor region having a second-type impurity complementary to said first-type impurity;

an upper semiconductor structure above said middle semiconductor region, wherein said upper semiconductor structure has a T-shape with a lower section and an upper section that is wider than said lower section;

spacers adjacent said lower section of said upper semiconductor structure and beneath said upper section of said upper semiconductor structure; and

a silicide layer adjacent said spacers and beneath said upper section of said upper semiconductor structure.

9. The device in claim 8, further comprising a dielectric structure over said middle semiconductor region and beneath said spacers.

10. The device in claim 9, wherein said middle semiconductor region is wider than said dielectric structure.

11. The device in claim 8, wherein said spacers separate said upper semiconductor structure from said silicide.

12. The device in claim 8, wherein said middle semiconductor region comprises:

an intrinsic middle semiconductor region; and

an extrinsic middle semiconductor region above said intrinsic middle semiconductor region.

13. The device in claim 8, wherein said spacers comprise insulators.

14. The device in claim 8, wherein said silicide comprises a salicide.

15. A method of making a transistor, said method comprising:

forming a extrinsic base above an intrinsic base;

protecting a portion of said extrinsic base using a sacrificial mask that is positioned over a center of said extrinsic base;

siliciding exposed portions of said extrinsic base, wherein said siliciding process leaves a non-silicided portion over said center of said extrinsic base;

forming an emitter opening through a center of said non-silicided portion of said extrinsic base;

forming spacers in said emitter opening; and

forming an emitter in said emitter opening,

wherein said spacers separate said emitter from silicided portions of said extrinsic base.

16. The method in claim 15, further comprising, before forming said extrinsic base:

patterning an insulator over said center of said intrinsic base; and

epitaxially growing said extrinsic base over said insulator and said intrinsic base.

17. The method in claim 16, wherein said process of epitaxially growing said extrinsic base grows polysilicon above said insulator and single crystal silicon above the exposed portions of said intrinsic base.

18. The method in claim 16, wherein said spacers are formed on said insulator.

19. The method in claim 15, wherein said siliciding process forms said silicided portions of said extrinsic base horizontally adjacent to said non-silicided portion.

20. The method in claim 15, further comprising, before forming said emitter opening, forming an insulator layer above said extrinsic base, wherein said emitter opening is formed through said insulator layer.

21. A method of making a transistor, said method comprising:

forming a lower semiconductor structure having a first-type impurity;

forming a middle semiconductor region above said lower semiconductor structure, said middle semiconductor region having a second-type impurity complementary to said first-type impurity;

protecting a portion of said middle semiconductor region using a sacrificial mask that is positioned over a center of said middle semiconductor region;

siliciding exposed portions of said middle semiconductor region, wherein said siliciding process leaves a non-silicided portion over said center of said middle semiconductor region;

forming an upper semiconductor structure opening through a center of said non-silicided portion of said middle semiconductor region;

forming spacers in said upper semiconductor structure opening; and

forming an upper semiconductor structure in said upper semiconductor structure opening,

wherein said spacers separate said upper semiconductor structure from silicided portions of said middle semiconductor region.

22. The method in claim 21, further comprising, before forming said middle semiconductor region:

forming a silicon layer over said lower semiconductor regions;

patterning an insulator over said center of said silicon layer; and

epitaxially growing said middle semiconductor region over said insulator and said silicon layer.

23. The method in claim 22, wherein said process of epitaxially growing said middle semiconductor region grows polysilicon above said insulator and single crystal silicon above the exposed portions of said silicon layer.

24. The method in claim 21, wherein said spacers are formed on said insulator.

25. The method in claim 21, wherein said siliciding process forms said silicided portions of said middle semiconductor region horizontally adjacent to said non-silicided portion.

26. The method in claim 21, further comprising, before forming said upper semiconductor structure opening, forming an insulator layer above said middle semiconductor region, wherein said upper semiconductor structure opening is formed through said insulator layer.

27. A method of making a bipolar complementary metal oxide semiconductor (BiCMOS) device, said method comprising:

forming a collector;

forming shallow trench isolation regions adjacent said collector;

forming an intrinsic base above said collector;

forming a raised extrinsic base above said intrinsic base;

protecting a portion of said extrinsic base using a sacrificial mask that is positioned over a center of said extrinsic base;

siliciding exposed portions of said extrinsic base, wherein said siliciding process leaves a non-silicided portion over said center of said extrinsic base;

forming an emitter opening through a center of said non-silicided portion of said extrinsic base;

forming spacers in said emitter opening; and

forming an emitter in said emitter opening,

wherein said spacers separate said emitter from silicided portions of said extrinsic base.

28. The method in claim 27, further comprising, before forming said extrinsic base:

patterning an insulator over said center of said intrinsic base; and

epitaxially growing said extrinsic base over said insulator and said instinsic base.

29. The method in claim 28, wherein said process of epitaxially growing said extrinsic base grows polysilicon above said insulator and single crystal silicon above the exposed portions of said intrinsic base.

30. The method in claim 27, wherein said siliciding process forms said silicided portions of said extrinsic base horizontally adjacent to said non-silicided portion.

31. The method in claim 27, wherein said spacers are formed on said insulator.